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Claims

1. A switching arrangement for the controlled parallel switching of a first energy-storing electrolytic condenser (C1) with a second energy-storing electrolyte condenser (C2) in response to a switching signal supplied to a control input (VS), said first electrolytic condenser (C1) has a capacity of at least 500 μF ; said second electrolytic condenser has a likewise large capacity, the switching arrangement comprises an electronic switch formed by the main circuit of a semiconductor device being a field effect transistor (FT) with a gate electrode connected through an RC-type delay member to the control input (VS);
- 10 characterized in that for protecting both the field effect transistor (FT) and the connected electrolytic condensers (C1, C2) from the damaging effect of current surges appearing as switching transients but which, at the same time, affects the switching process only to the extent necessary for the protection, the rising of the current in said main circuit is delayed, wherein the delay is provided by two delay members, the first delay member is constituted
- 15 by said RC-type delay member, the second delay member being an inductive element (L) connected in the main circuit of the field effect transistor (FT), the inductive element (L) has a very low ohmic resistance and being constituted by a conductor (10) of predetermined length surrounded by a high-frequency ferrite core (11, 12); the delay effected by the RC member ensures only a fraction of the full switching delay.
- 20 2. The switching arrangement as defined in claim 1, characterized in that the ferrite core (11, 12) has two bores which are at a predetermined distance from one another and which have parallel axes; the conductor (10) has two legs passed through the bores.
3. The switching arrangement as defined in claim 2, characterized in that it comprises a plurality of short, stacked ferrite cores (11).
- 25 4. The switching arrangement as defined in claim 1, characterized in that in the RC member the capacitive element is formed by the input capacity of the field effect transistor (FT) and the unavoidable scattered capacities.
5. The switching arrangement as defined in claim 1, characterized in that the capacity of the switched electrolytic condensers is in the range of 10,000 μF .

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INTERNATIONAL SEARCH REPORT

 International Application No
 PCT/HU2005/000017

 A. CLASSIFICATION OF SUBJECT MATTER
 IPC 7 H02H9/00 H01F17/06

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

 Minimum documentation searched (classification system followed by classification symbols)
 IPC 7 H02H H01F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the International search (name of data base and, where practical, search terms used)

EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 122 724 A (CRISS ET AL) 16 June 1992 (1992-06-16)	1,5
Y	claims 1,2; figure 1	2-4
Y	US 4 656 451 A (POMPONIO ET AL) 7 April 1987 (1987-04-07) figures 2,4	2,3
Y	ANONYMOUS: "Advanced Design System 2002 - Circuit Components Nonlinear Devices" 'Online! 1 February 2002 (2002-02-01), AGILENT TECHNOLOGIES, XP002330952 Retrieved from the Internet: URL: http://eesof.tm.agilent.com/docs/adsdoc2002/pdf/ccnld.pdf 'retrieved on 2005-06-08! Describes a model of the FET pages 6-9 - pages 6-10	4

☐ Further documents are listed in the continuation of box C.


Patent family members are listed in annex.

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Date of the actual completion of the International search

15 June 2005

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No

PCT/HU2005/000017

Patent document cited in search report		Publication date	Patent family member(s)	Publication date
US 5122724	A	16-06-1992	NONE	
US 4656451	A	07-04-1987	NONE	